frLabel

Specification

Frame Labeling Core

Revision 1.0

14 July 2025

English ver.

1. Overview

1.1. Introduction

- The **Frame Labeling Core** (hereafter referred to as *frLabel*) is an embedded core that analyzes the connectivity of a source image and assigns ascending numbers to each connected group, outputting the results as a destination image.
  You can select either **4-connectivity** or **8-connectivity** for the analysis.
- The analysis results are stored in memory as 16-bit IDs.
  Even if the IDs are different, they may still belong to the same connected group (label).
  The mapping of which ID belongs to which label is also stored in memory.
  By replacing the IDs according to their corresponding labels, a fully labeled result can be obtained.
- For each label, the system manages values such as the **number of pixels**, **perimeter length**, **minimum and maximum coordinates**, and the **Euler characteristic**.
- Using these managed values, filtering can be applied to perform labeling based on specific conditions.
- IDs start from 1, and the maximum supported value is **65,535**.
  Any values exceeding 65,535 cannot be labeled correctly.
- A special type of labeling using **two threshold values** is also supported.
  It outputs a binary result of **true (1)** or **false (0)**.
  Pixels are divided into labeled and unlabeled regions, and those in the intermediate region are labeled as true only if they are adjacent to already labeled pixels.
  This is used for **hysteresis thresholding** in the **Canny filter**.

  Note: The memory interface (I/F) needs to be customized according to the system.

1.2. Main Parameters

- **Memory Bus**
  Data Read/Write: 64-bit × 4
  Command List Read: 64-bit × 1
- **Throughput**
  1 pixel per cycle
- **Pixel Format**
  - 8-bit component (grayscale)
  - 16-bit component (RGB565, ARGB1555)

- 24-bit component (RGB888, read-only supported)
- 32-bit component (ARGB8888)

- **Maximum Labels**

  65,535

- **Clock**

  Undefined (depends on implementation process)

1.3. Implementation Parameters

Parameter Name	Description	Default Value
BLR	• Radix of burst length of externa(parameter) bus • Sets the burst unit for 64-bit memory access	1(4 以下)
BSR	• Radix of burst length of data bus • Sets the burst unit for 64-bit memory access	1(4 以下)

2. Signal Lines

2.1. Control Bus Interface

Signal Name	IO	Pol	Source	Description
cntlReq	I	+	clk	• Request signal • Evaluate cntlGnt
cntlGnt	O	+	clk	• Grant signal
cntlRxw	I	+	clk	• R/W signal • Evaluate cntlReq & cntlGnt 0: Write 1: Read
cntlAddr[31:0]	I	+	clk	• Address signal • Evaluate cntlReq & cntlGnt
cntlWrAck	O	+	clk	• Writ acknowledge signal
cntlWrData[31:0]	I	+	clk	• Write data signal • Evaluate cntlWrAck
cntlRdAck	O	+	clk	• Read acknowledge signal
cntlRdData[31:0]	O	+	clk	• Read data signal • Sync cntlRdAck
cntlIrq	O	+	clk	• Interrupt signal

				• Level hold type

2.2. PSS Interface

Signal Name	IO	Pol	Source	Description
iVld	I	+	clk	• Pipeline start valid signal
iStall	O	+	clk	• Pipeline start stall signal
iEnd[1:0]	I	+	clk	• Pipeline end signal • LSB is x coodinate end • MSB is y coodinate end
iAddr[31:0]	I	+	clk	• Address to fetch context data • Evaluate iVld & !iStall
iDelta[15:0]	I	+	clk	• Transfer volume • Evaluate iVld & !iStall
iIndex[64:0]	I	+	clk	• Five coodinates to specify the processing • Evaluate iVld & !iStall
oVld	O	+	clk	• Pipeline end valid signal
oStall	I	+	clk	• Pipeline end stall signal

2.3. Memory Interface0-2(Data R/W Use)

Signal Name	IO	Pol	Source	Description
miReq	O	+	clk	• Request signal
miGnt	I	+	clk	• Grant signal
miRxw	O	+	clk	• R/W signal
miAddr[31:0]	O	+	clk	• Address signal
miRdStrb	O	+	clk	• Read strobe
miRdAck	I	+	clk	• Read acknowledge signal
miRdData[63:0]	I	+	clk	• Read data signal
miWrStrb	O	+	clk	• Write strobe signal
miWrAck	I	+	clk	• Write acknowledge signal
miWrData[63:0]	O	+	clk	• Write data signal
miWrMask[7:0]	O	+	clk	• Write mask signal

2.4. Memory Interface(Parameter Read Use)

Signal Name	IO	Pol	Source	Description

meReq	O	+	clk	• Request signal
meGnt	I	+	clk	• Grant signal
meAddr[31:0]	O	+	clk	• Address signal
meStrb	O	+	clk	• Read strobe signal
meAck	I	+	clk	• Read acknowledge signal
meData[63:0]	I	+	clk	• Read data signal

2.5. Utillity

Signal Name	IO	Pol	Source	Description
rstReq	O	+	clk	• Internal reset signal to reset the external system
rstAck	I	+	clk	• Acknowledge of rstReq
fReq	I	+	clk	• 1 clock early request against the iVld signal • Use to generate gate signal (for pss)
pReq	O	+	clk	• 1 clock early request against the all memory access signal • Use to generate gate signal (for memory)
gate	O	+	clk	• Gated clock control signal signifying condition of each internal block
gclk	I	+	clk	• Gated clock
clk	I	＋	clk	• Clock
reset_n	I	-	-	• Asynchronous reset signal

3. Structure and Operational Description

3.1. Structural Overview

- The Pipeline Slice Scheduler (hereafter *pss*) retrieves the necessary context from memory, generates information such as coordinates, and activates the *frLabel*.
  For more details, refer to the *pss* specification document.
  Note that since the connection interface is simple, using *pss* is not mandatory.
  In such cases, replace the role of *pss* with your own custom core.
- *frLabel* operates as a pipeline, as illustrated in Figure 1.
  The Initiator fetches parameters from the command list in memory and handles overall control.

The data is repeatedly read from memory, processed, and output, while also performing statistical operations such as the accumulation of the number of pixels and coordinates (centroid) per label.

- The system performs ID generation and labeling (Judge) based on the states of neighboring pixels, as well as label sorting (Sort).
  IDs belonging to the same label can be remapped using functions in other engines (e.g., *Blt*) to produce a fully labeled image.

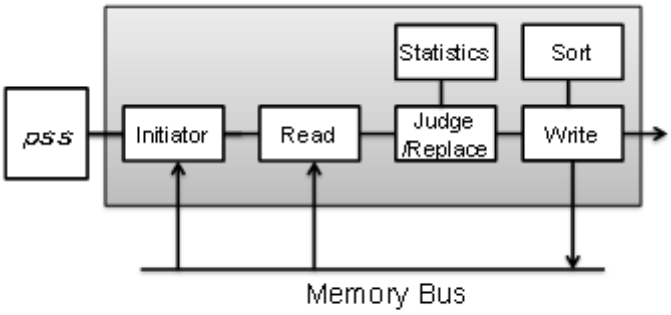


Figure 1 *frLabel* Block Diagram

3.2. Operational Overview

- The pss scans destination coordinates along an arbitrary axis and sends the results to the Initiator.
  Settings for the pss (such as image information and processing units) must be preloaded into memory.
  The pss time-division manages up to 256 different configurations (depending on the implementation), and after scheduling, it activates *frLabel*.
- The Initiator reads the context containing the image information provided by the pss and performs the initial setup of the pipeline.
  Since processing is limited to frame units, the context is only read from memory at the beginning of each frame.
- After scanning the entire image and storing IDs in memory, labels are generated.
  Labels are ascending values derived from the IDs found during image scanning.
  At this point, labeling can be selectively applied based on criteria such as the number of pixels per label.
- Temporary data and the label table are deployed in memory, so sufficient memory space must be allocated.
- Input/output data must reside in cache memory.
  Refer to the memory controller specification for how to configure cache memory usage.

3.3. Input/Output Format

- The pixel data in memory supports the following formats.

  Only read access is supported.

Bit/Word	Component	Description
8	A or R or G or B	• Assigned to all elements of the ARGB pipeline
16	ARGB or RGB	• For ARGB, the 1, 5, 5, and 5-bit components are each expanded to 8 bits • For RGB, the 5, 6, and 5-bit components are each expanded to 8 bits (A is forcibly set to 0xFF) • In the expansion process, any deficit in the LSB direction is filled by copying bits from the MSB direction
24	RGB	• For RGB, the 8, 8, 8-bit components are assigned (A is forcibly set to 0xFF)
32	ARGB	• For ARGB, the 8, 8, 8, and 8-bit components are assigned

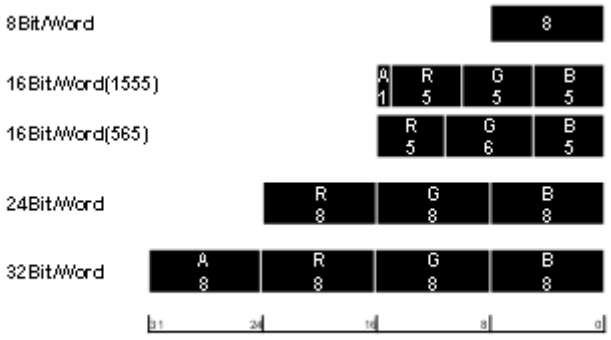


Figure 2 Pixel Format(ARGB)

The following formats are supported for IDs and labels.

Bit/Word	Description
16	• Outputs 16-bit labels、max=FFFFh=65535d

3.4. Labeling Targets

- In Normal Mode (Mode 0), input pixel data is filtered using a specified color and mask.
  Unused information is removed via the mask, and only pixels that match the specified color become the targets for labeling.
  Pixels with a value of 0 can also be included as targets.
- In Threshold Mode (Mode 1), two thresholds—upper and lower—are set.
  Pixels are considered for labeling if any of their components fall between these thresholds.
  The lower bound is inclusive, while the upper bound is exclusive.
  If the upper bound is set to 0, that component is ignored in the evaluation.
  This mode is used to exclude unnecessary components from labeling.
- Min (Mode 2) and Max (Mode 3) modes also use upper and lower thresholds.
  Values falling between the thresholds (inclusive of the lower, exclusive of the upper) are categorized into an intermediate zone.
  In Min Mode, values less than or equal to the lower threshold are forcibly assigned label ID 1,
  while values greater than or equal to the upper threshold (exclusive) are assigned label ID 0.
  In Max Mode, the assignments are reversed.
  Normal labeling is performed for the intermediate zone,
  but in the end, regions that are not connected to label 1 are converted to 0, and connected ones to 1.

3.5. Label Limitations

- Since the data format for both IDs and labels is 16 bits, only values from 1 to 65,535 can be assigned.
  Any values exceeding this range will be forcibly set to label value 65,535, which does not represent a valid label.
  As long as the assigned number of labels (IDMax) remains below 65,535, the result is considered valid.
- Detection of values exceeding 65,535 is possible by setting ThOver in the Info Register and InfoEn Register.
  An interrupt will continue to be triggered as long as the value exceeds 65,535.
  After processing all input pixels, a reset can be performed to restart the operation.

3.6. Algorithm

- A hardware-oriented algorithm based on image scanning is employed.
  To minimize memory access, only two directions opposite to the scan (i.e., toward smaller X and Y coordinates) are used when referencing adjacent pixels.
- ID assignment varies depending on whether 4-connectivity or 8-connectivity is used.
  8-connectivity increases the frequency of memory access.
- IDs are assigned in ascending order starting from 1.
  Evaluation proceeds in order from smaller Y-coordinates due to XY coordinate scanning.
  The evaluation references three results: the previously evaluated result at coordinate X-1, the past result at Y-1, and the results at both X-1 and Y-1.
  Evaluation results are stored in memory as 2-byte words, sized to the image dimensions, as the Destination data.
- Simultaneously with the Destination data, a 2-byte Work data word is generated to establish correspondence between IDs and labels.
  The offset from the base address of the Work region represents the ID, and the address stores the corresponding label.
- The Work region requires a maximum of 0x10000 × 2 bytes = 128 kB + 8 kB.
- Optional Metric data can be generated for label measurements.
  These include: area, number of holes (Euler characteristic), edge contact, perimeter, bounding box values, and coordinate accumulation (L1 norm).
- Based on the Metric data, Mark data can be generated.
  The Mark data selects only the necessary labels according to specified filter information.
  New labels are reindexed in ascending order starting from 1.
  After converting the Destination data into labels using the Work data, the labels can be further remapped using the Mark data to assign new labels.
- Labels can be filtered using various management values to retain only those that meet specific conditions.
  These management values include area (pixel count), perimeter, minimum and maximum pixel values, and number of holes (Euler characteristic).
- Conversion from the Destination data to the final output is performed using a separate engine that supports remapping functionality.

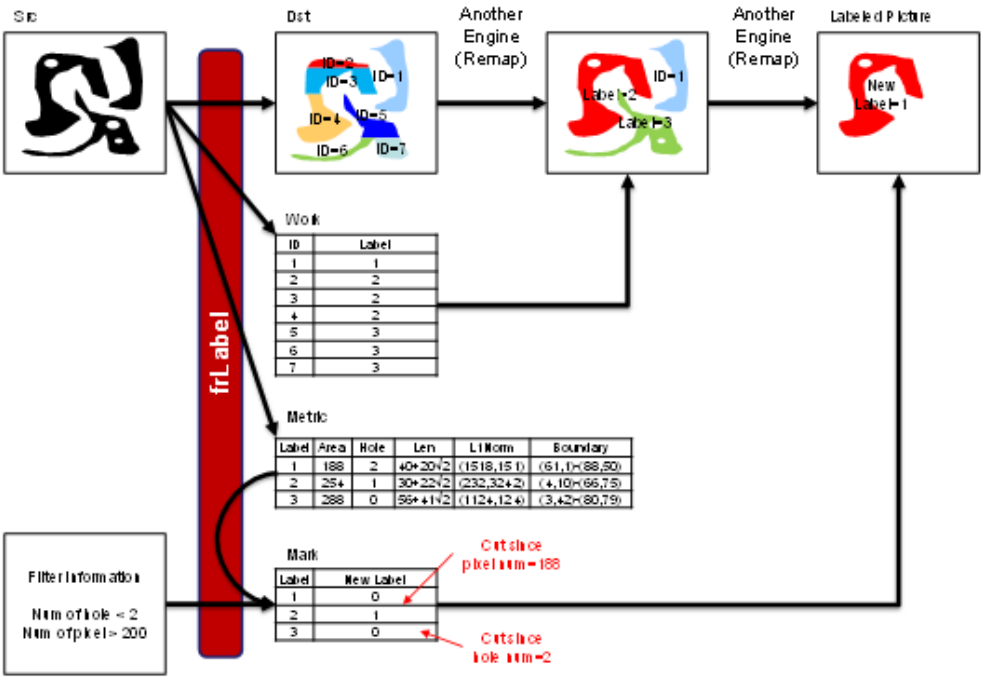


Figure 3 Labeling Process

3.7. Connection with *pss*

- The command list is retrieved from memory based on the address (iAddr) output by the pss.

  For details on the command list format, refer to the command list documentation.

  If the pss is not present, access the pss interface directly.
- Using the coordinate (iIndex) output by the pss and the parameters within the command list,

  the starting addresses of the input and output image data are calculated.

  Zero-order coordinates are not used.

  The initial address is determined using the following formula:

  Here, Y and Z represent the first- and second-order coordinates,

  and StrideY and StrideZ represent step sizes for each coordinate axis (the units vary depending on the format).

  Whether Y and Z are referenced, and how the strides are set, is determined by the addressing mode.

$$\text{StartAddress} = \text{BaseAddress} + (\text{Stride}_Y \times Y) + (\text{Stride}_Z \times Z)$$

Normally, data is read/written by incrementing the address in memory word units.
In contrast, in transpose mode, data is read/written by adding the stride value.

As with calculating the initial address, these settings are defined via the addressing mode.
In general, non-transposed access yields better memory performance.
Fragmentation by pss is possible; however, insertion of other tasks is prohibited, making it practically ineffective.
This restriction exists because *frLabel* employs a frame-based processing algorithm specific to its architecture.
Therefore, it is not possible to insert another frame-processing task between ongoing frame processes.

3.8. Performance

- Label assignment is performed at 1 pixel per cycle.
- In principle, the image is scanned along XY coordinates, resulting in sequential memory access where addresses are incremented continuously.
  However, since some past results are referenced during processing, there may be localized random access depending on the image content.

4. Register Description

4.1. Overview

- Each register is accessed via the control bus.
- Some registers may affect pipeline operation and performance, so care must be taken regarding the timing of their configuration.
- In the detailed register descriptions, the following symbols are used to indicate access types:
  R – Read Only (writes have no effect)
  R/W – Read / Write
  R/WC – Read / Write, Clear on Write
- Do not access reserved registers. Also, when writing to reserved fields, always set them to '0'.
- In address and data fields, **'x'** denotes a "don't care" value.

4.2. Definition

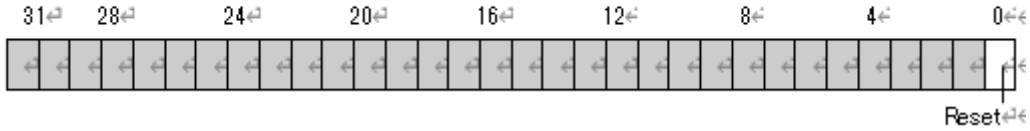
Address	Register Name	Description
0000_0000	Reset	Reset control

0000_0004	System	System ontrol
0000_0008	Info	Information
0000_000c	IntEn	Interrupt accept

4.3. Details

▪ 4.3.1.1. Reset Register

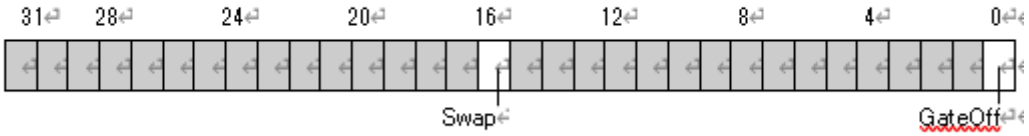
[Address: 0x0000_0000]



Name	Type	Default	Description
Reset	R/W	0	**Synchronous Reset** After setting to '1', it must be cleared by setting to '0'. Unlike the reset_n signal, the contents of the registers are retained. After setting to '1', the rstReq signal is immediately asserted. This signal notifies external components that *frLabel* has entered a reset state and requests appropriate handling. Once the handling is complete, the rstAck signal must be asserted (if no handling is needed, rstAck should always be asserted as '1'). After these procedures are completed, the **Reset** signal automatically returns to '0'.

▪ 4.3.1.2. System Register

[Address: 0x0000_0004]

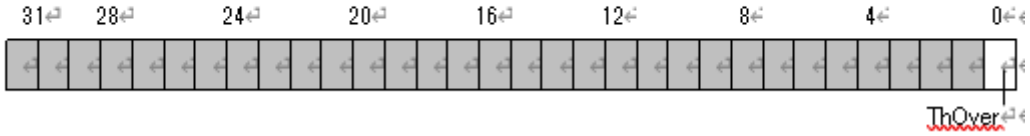


Name	Type	Default	Description
Swap	R/W	0	**Word Swap Setting** When set to '1', the upper 32 bits and lower 32 bits of the 64-bit bus are swapped.

			Swapping within each 32-bit word is specified in the command list.
GateOff	R/W	0	**Gated Clock Off Mode** When set to '1', all bits of the gate signal are fixed to '1'.

▪ 4.3.1.3. Info Register

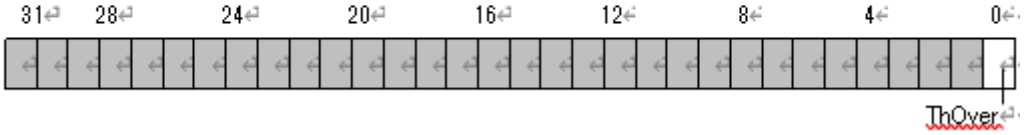
[Address: 0x0000_0008]



Name	Type	Default	Description
ThOver	R/W	0	Indicates that the number of assigned IDs (labels) has exceeded the threshold. It is automatically cleared after *frLabel* is activated.

▪ 4.3.1.4. IntEn Register

[Address: 0x0000_000c]



Name	Type	Default	Description
ThOver	R/W	0	When set to '1', enables interrupts when the ThOver bit in the IntStat register is set to '1'.

5. Command List Description

5.1. Overview

- The **command list** has its starting address specified by the address value output from the **pss**.
  After *frLabel* is activated, it retrieves the command list and stores it into internal registers.
- The command list is managed completely independently at each stage within the pipeline. This enables each stage to operate independently with different command lists, even during pipeline operation.
  Therefore, synchronization commands are not required.

- For all **reserved registers and fields**, a value of '0' must be set.
- The addresses shown are **relative addresses** from the address value output by the pss.

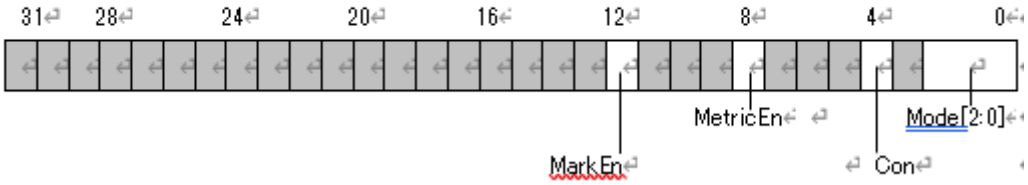
5.2. Definition

Address	Command Name	Description
00	Cntl	Global Control
04	–	Reserved
08	Color/Lower	Target Color / Lower Threshold
0c	Mask/Upper	Mask / Upper Threshold
10	FFilter0	Filter Configuration 0 (Front)
14	FFilter1	Filter Configuration 1 (Front)
18	BFilter0	Filter Configuration 0 (Back)
1c	FBilter1	Filter Configuration 1 (Back)
20	SrcInfo	Source infomation
24	SrcBase	Source base address
28	DstInfo	Destination infomation
2c	DstBase	Destination base address
30	MetricBase	Metric Information Base Address
34	MarkBase	Label Information Base Address
38	WorkBase	Workl Information Base Address
3c	Size	Source size

5.3. Details

▪ 5.3.1.1. Cntl Command

[Address: 0x00]



Name	Description
MarkEn	hen set to '1', generates **mark information (labels)** corresponding to **work information (IDs)**. Setting MetricEn to 2 or 3 is required. By searching the mark information using an ID, the label to which that ID

belongs can be obtained.

MetricEn　　Configures measurement information for each **label** (not for ID).

The following measurements are performed:

	Description
Area[31:0]	Pixel Count
Edge[3:0]	Edge Contact Information (from LSB: left, right, top, bottom)
Len0[23:0] Len1[23:0]	Perimeter is calculated as: Len0 + $\sqrt{2}$ × Len1 Includes the perimeter of enclosed holes as well.
EC[27:0]	Number of Holes and Euler Characteristic are calculated as: 1 − EC
Vmax[7:0] Vmin[7:0]	Maximum and Minimum Pixel Values
Xmin[15:0] Ymin[15:0] Xmax[15:0] Ymax[15:0]	Maximum and Minimum Coordinates
Xsigma[31:0] Ysigma[31:0]	Accumulated Coordinate Values (L1 Norm) Dividing by the pixel count yields the centroid position.

Con　　Configures the connectivity method:

'0' for 4−connectivity, '1' for 8−connectivity.

Mode　　Configures t

Mode	Description
0	Normal Mode Labeling is performed by setting the target pixel color in Color and the pixel mask value in Mask.
1	Threshold Mode Labeling is performed by setting the lower threshold in Color and the upper threshold in Mask.
2	Min Mode Labeling is performed by setting the lower threshold in Color and the upper threshold in Mask.

	Based on pixel comparison, three regions are defined (Low, Mid, High), and the following processing is applied:
	• Low region: Assigned ID value 1
	• High region: Assigned ID value 0
	• Mid region:
	  ○ Pixels adjacent to ID value 1 are assigned 1
	  ○ All others are assigned values 2 or greater

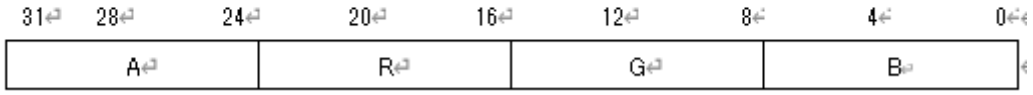
3	Max Mode
	Labeling is performed by setting the lower threshold in Color and the upper threshold in Mask.
	Based on pixel comparison, three regions are defined (Low, Mid, High), and the following processing is applied:
	• Low region: Assigned ID value 0
	• High region: Assigned ID value 1
	• Mid region:
	  ○ Pixels adjacent to ID value 1 are assigned 1
	  ○ All others are assigned values 2 or greater

4	In Mode 0, labeling is performed not only on pixels that evaluate as true (as determined by Color/Mask), but also simultaneously on those that evaluate as false.
5	In Mode 1, labeling is performed not only on pixels that evaluate as true (as determined by Color/Mask), but also simultaneously on those that evaluate as false.
6	In Mode 2, labeling is performed not only on pixels that evaluate as true (as determined by Color/Mask), but also simultaneously on those that evaluate as false
7	In Mode 3, labeling is performed not only on pixels that evaluate as true (as determined by Color/Mask), but also

	simultaneously on those that evaluate as false

▪ 5.3.1.2. Color/Lower Command

[Address: 0x08]

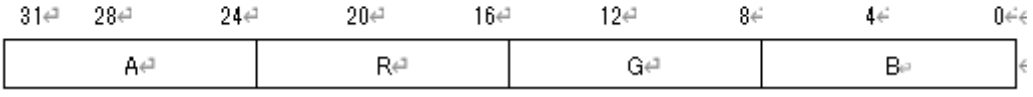


Name	Description
A, R, G, B	The function varies depending on the Mode of the Cntl Command.

Cntl.Mode	Description
0,4	**Normal Mode** Sets the target pixel values. The value from the **Mask Command** is also relevant. Labeling is applied when **all elements** satisfy the condition (i.e., the evaluation result is true for all components).
1,2,3, 5,6,7	**Threshold / Min / Max Mode** Sets the **lower bound** of the target pixel values. If set to 0, the evaluation for that component is disabled. Labeling is applied when **any one** of the components satisfies the condition (i.e., the evaluation result is true for at least one component).

▪ 5.3.1.3. Mask/Upper Command

[Address: 0x0c]



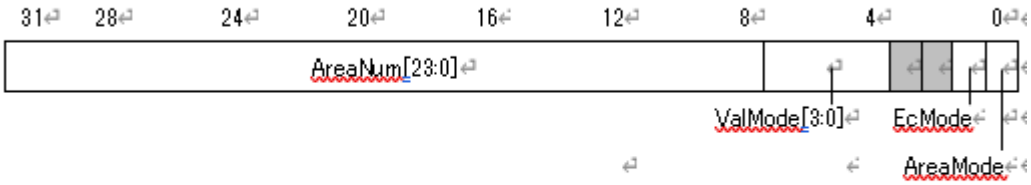
Name	Description
A, R, G, B	The function varies depending on the **Mode** of the **Cntl Command**.

Cntl.Mode	Description
0,4	**Normal Mode** Sets the **mask** for the target pixel values. The value from the **Color Command** is also relevant.
1,2,3, 5,6,7	**Threshold / Min / Max Mode** Sets the **upper bound** of the target pixel values.

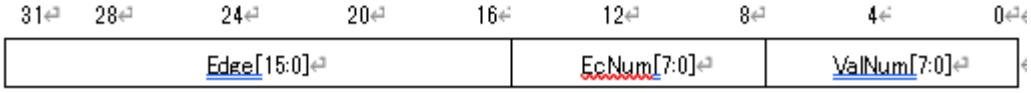
	If set to 0, upper bound evaluation for that component is not performed.

▪ 5.3.1.4. FFilter0,1 Command

[Address: 0x10]



[Address: 0x14]



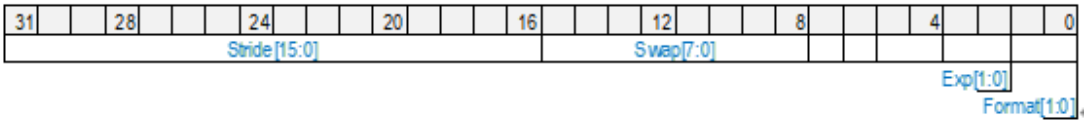
Name	Description
AreaNum	Sets the **pixel count (area)** to be referenced by the filter.
ValMode	Sets filter conditions based on **pixel values**. A judgment flag is generated using the comparison results between the maximum pixel value ValMax in the label and ValNum (EvalMax), and similarly between the minimum pixel value ValMin and ValNum (EvalMin). Flag = ValMode[{EvalMax, EvalMin}] Where: EvalMax = ValMax< ValNum、EvalMin = ValMin< ValNum Note: If ValNum is 0, the evaluation is disabled.
EcMode	Sets filter conditions based on the Euler characteristic. A judgment flag is generated from the comparison between the number of holes EC within the label and the threshold value ECNum. Flag = Area< ECNum When ECMode = 0 Flag = Area≧ECNum When ECMode = 1 However, if ECNum is 0, the evaluation is disabled.
AreaMode	Sets filter conditions based on pixel count (AreaNum). A judgment flag is generated from the comparison between the number of pixels (Area) within the label and AreaNum. Flag = Area< AreaNum When AreaMode = 0

Flag = Area≧AreaNum When AreaMode = 1

However, if AreaNum is 0, the evaluation is disabled.

▪ 5.3.1.5. SrcInfo Command

[Address: 0x20]



Name	Description
Stride	Sets the address of the **Source data** to 'update width – 1'. The unit depends on the **Format**.
Swap	Configures **byte swap** for the referenced **Source data**. A byte-level mapping is performed from input data In[31:0] to internal data Pipe[31:0]. Be careful: if the configuration is not one-to-one, unknown values or overlapping may occur.
Exp	Configures the detailed **pixel format** of the **Source data** (see **Format** for details).
Format	Sets the **Bpp (Bits per Pixel)** for the **Source data** pixel format.

Value	Swap[7:6]	Swap[5:4]	Swap[3:2]	Swap[1:0]
	Pipe[31:24]	Pipe[23:16]	Pipe[15:8]	Pipe[7:0]
0	In[31:24]	In[23:16]	In[15:8]	In[7:0]
1	In[7:0]	In[31:24]	In[23:16]	In[15:8]
2	In[15:8]	In[7:0]	In[31:24]	In[23:16]
3	In[23:16]	In[15:8]	In[7:0]	In[31:24]

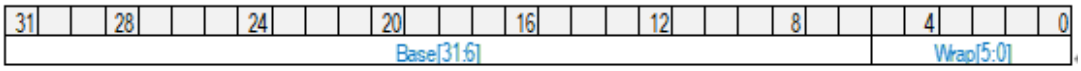
Format	Exp	Pipe [31:24]	Pipe [23:16]	Pipe [15:8]	Pipe [7:0]	Note
0 1Bpp	3	Internal Special				Use Distance Filter Only
0 8Bpp	1–3	In[7:0]				8bit Replica
1 16Bpp	0	Gray	In [15:11] [15:13]	In [10:5] [10:9]	In [4:0] [4:2]	RGB565 Lower Replica
	1–3					Reserved
2 24Bpp	0	In [23:16]	In [23:16]	In [15:8]	In [7:0]	
	1	Gray	In [23:16]	In [15:8]	In [7:0]	

	2	0xff	In [23:16]	In [15:8]	In [7:0]	Alpha=1.0
	3	Gray	Gray	Gray	Gray	All Gray
3 32Bpp	0	In [31:24]	In [23:16]	In [15:8]	In [7:0]	
	1	Gray	In [23:16]	In [15:8]	In [7:0]	
	2	0xff	In [23:16]	In [15:8]	In [7:0]	Alpha=1.0
	3	Gray	Gray	Gray	Gray	All Gray

In: Memory side
Pipe: Processing side (=ARGB)
Gray: (2 In[23:16] + 5 In[15:8] + In[7:0]) / 8

▪ 5.3.1.6. SrcBase Command

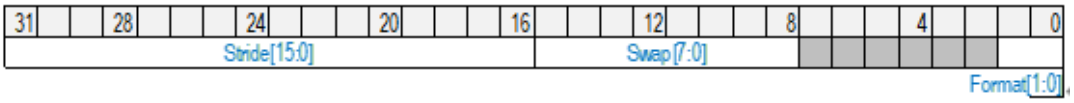
[Address: 0x24]



Name	Description
Base	Sets the base address of the Source data. Must be aligned to a 64-byte boundary.
Wrap	By setting the MSB to '1', the 4-bit address mask can be specified using Wrap[4:1]. This setting is applicable only when using cache. The mask value applied to the 32-bit address is: 0x007FFFFF >> ~Wrap[4:1] Additionally, the LSB of the address will transmit Wrap[0] as a 1-bit signal to the memory system. If the MSB is '0', no masking is performed, and the lowest 2 bits (Wrap[1:0]) are sent as information to the memory system via the LSB of the address. If Wrap[4:1] is '0', the lower 8 bits are valid, and the upper 24 bits are masked to 0. If Wrap[4:1] is 'F', the lower 23 bits are valid, and the upper 9 bits are masked to 0.

▪ 5.3.1.7. DstInfo Command

[Address: 0x60]

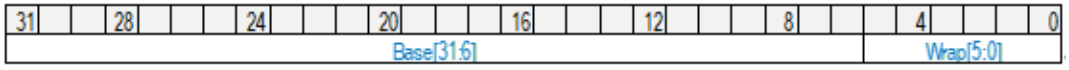


Name	Description
Stride	Sets the address of the Destination data to 'update width – 1'. The format is fixed at 2 bytes.
Swap	Configures byte swap for the Destination data.
Format	Sets the Bpp (Bits per Pixel) for the Destination data pixel format.

Format	Out [31:24]	Out [23:16]	Out [15:8]	Out [7:0]	Note
0 8Bpp				Pipe [7:0]	Upper Byte cut
1 16Bpp			Pipe [15:0]		
2 Reserved					
3 32Bpp	0	0	Pipe [15:0]		

▪ 5.3.1.8. DstBase Command

[Address: 0x2c]



Name	Description
Base	Sets the base address of the Destination data. It must be aligned to a 64-byte boundary, and the format is fixed at 2 bytes.
Wrap	By setting SB to '1', the 4-bit address mask is specified using Wrap[4:1]. This setting is limited to cache usage. The mask value applied to the 32-bit address is: 0x007FFFFF >> ~Wrap[4:1]. Additionally, Wrap[0] is sent as a 1-bit signal via the LSB of the address to the memory system. If the MSB is '0', no masking is applied, and Wrap[1:0] is sent as a 2-bit

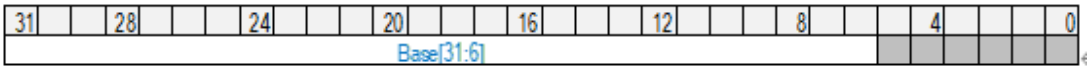
signal via the LSB of the address to the memory system.

If Wrap[4:1] is '0', the lower 8 bits are valid and the upper 24 bits are masked to 0.

If Wrap[4:1] is 'F', the lower 23 bits are valid and the upper 9 bits are masked to 0.

▪ 5.3.1.9. MetricBase Command

[Address: 0x30]



Name	Description
Base	Sets the **base address** of the **Metric (measurement) data**. It must be aligned to a **64-byte boundary**, and the format is **fixed at 32 bytes**. The **first word** contains the number of labels, followed by the **measurement information** for each label starting from label 1.

first Word:

	63 48	47 32	31 16	15 0
[255:192]				
[191:128]				
[127:64]				
[63:0]		PreNum [15:0]		FinalNum [15:0]

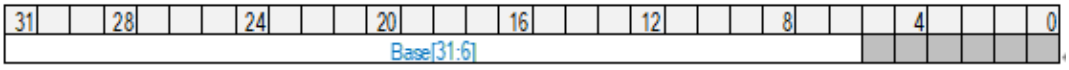
After the First Word :

	63 48	47 32	31 16	15 0
[255:192]	Ysigma[31:0]		Xsigma[31:0]	
[191:128]	Ymax[15:0]	Xmax[15:0]	Ymin[15:0]	Xmin[15:0]
[127:64]	Vmax Vmin	Len1[23:0]		Len0[23:0]
[63:0]	EC[27:0]	Edge	Area[31:0]	

Cntl.MetricEn referrence

▪ 5.3.1.10. MarkBase Command

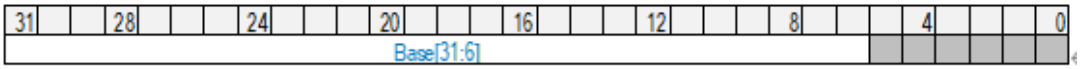
[Address: 0x34]



Name	Description
Base	Sets the **base address** of the **Mark data** (labels after filtering). It must be aligned to a **64-byte boundary**, and the format is **fixed at 2 bytes**. A value of '0' in the **Mark data** indicates **no label**.

▪ 5.3.1.11. WorkBase Command

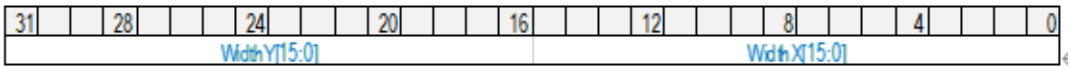
[Address: 0x38]



Name	Description
Base	Sets the base address of the Work data (labels corresponding to IDs). It must be aligned to a 64-byte boundary, and the format is fixed at 2 bytes. Requires up to 136 KB of memory allocation.

▪ 5.3.1.12. Size Command

[Address: 0x3c]



Name	Description
WidthY,X	Configures the write range in Source in units of pixels. Pixels beyond the boundary are treated as 0. A value of 0 represents infinity. Additionally, when the value is 0, edge detection is not performed except for X = 0 or Y = 0, and perimeter is not counted.